

Revision : 1.01

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25	AUDIO JACK

[illegible]

Model Name:GA-890XA-UD3

Component value change history

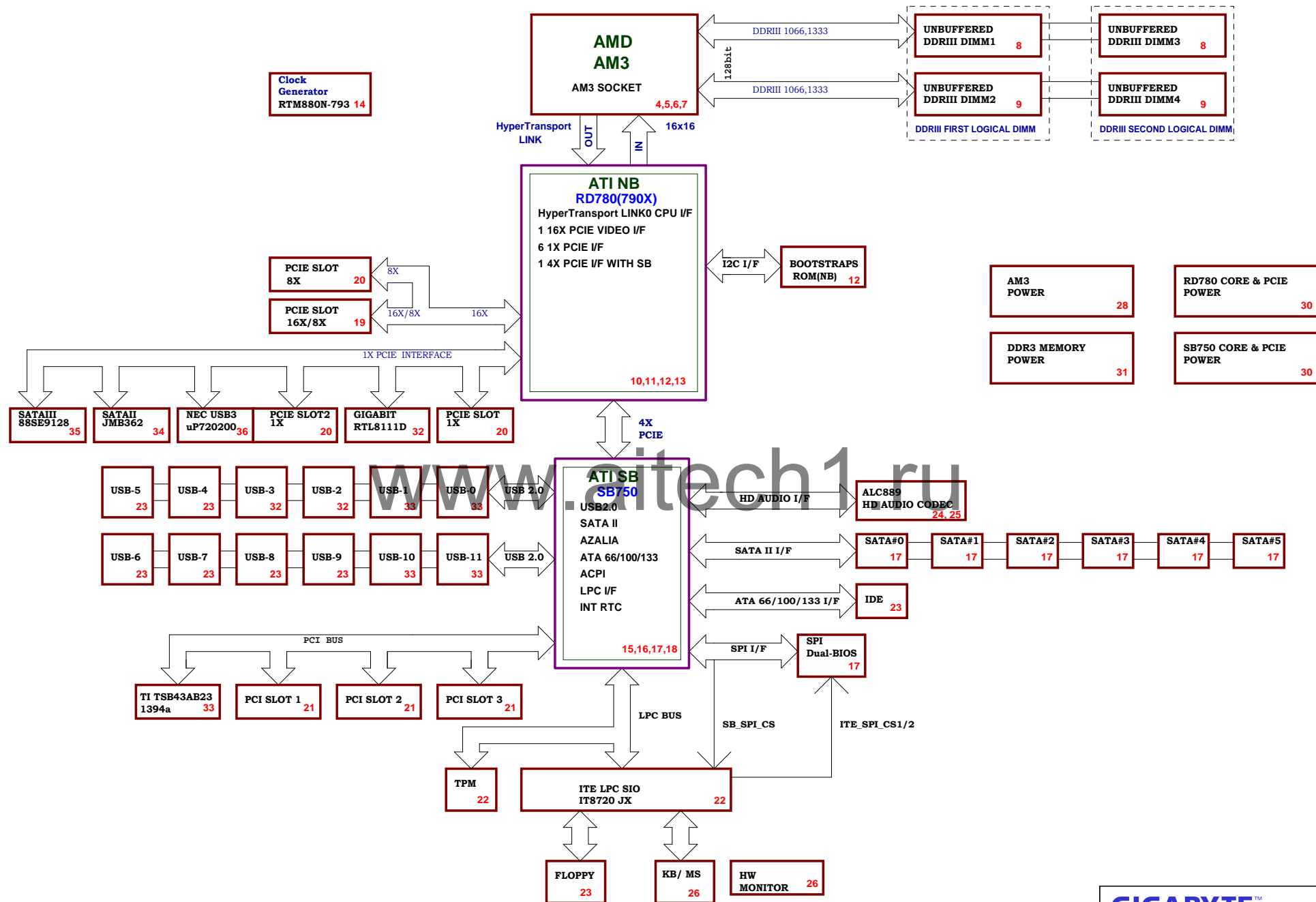
Version: 1.01

P-Code: U98094-0

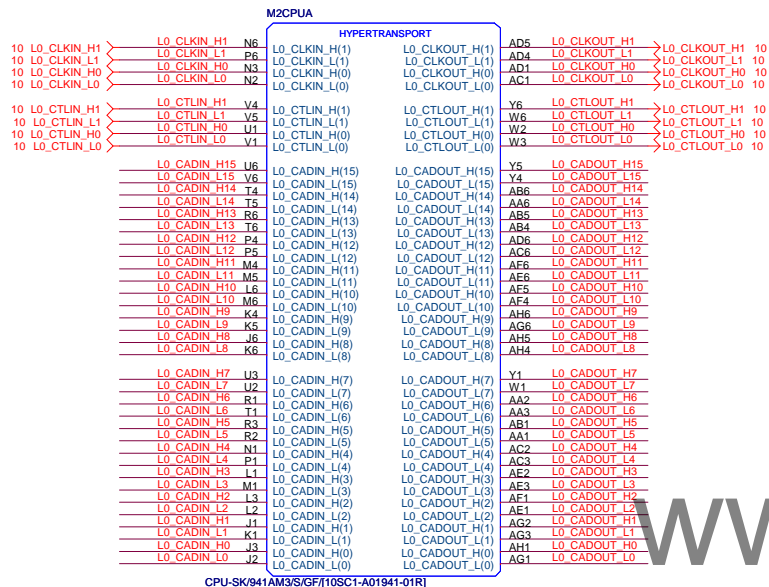
[illegible]

Circuit or PCB layout change for next version

[illegible]



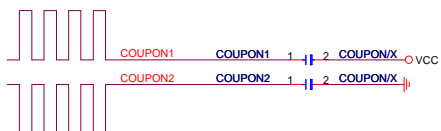
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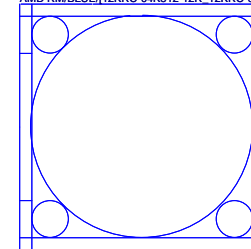
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CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

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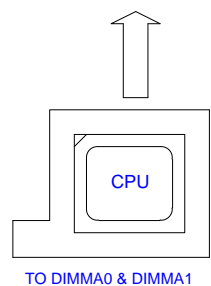


M2CPU
AMD RM/BLUE/12KRC-04K812-12R_12KRC-04K812-13R]

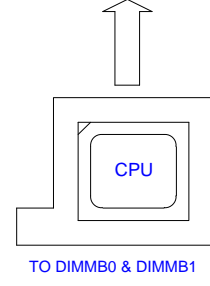
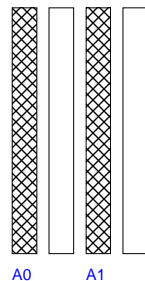


GIGABYTE™

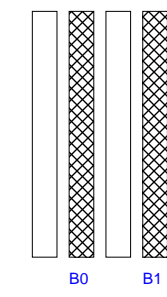
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Size	Document Number	Rev	
Custom	GA-890XA-UD3	1.01	
Date:	Friday, February 26, 2010	Sheet	4 of 35



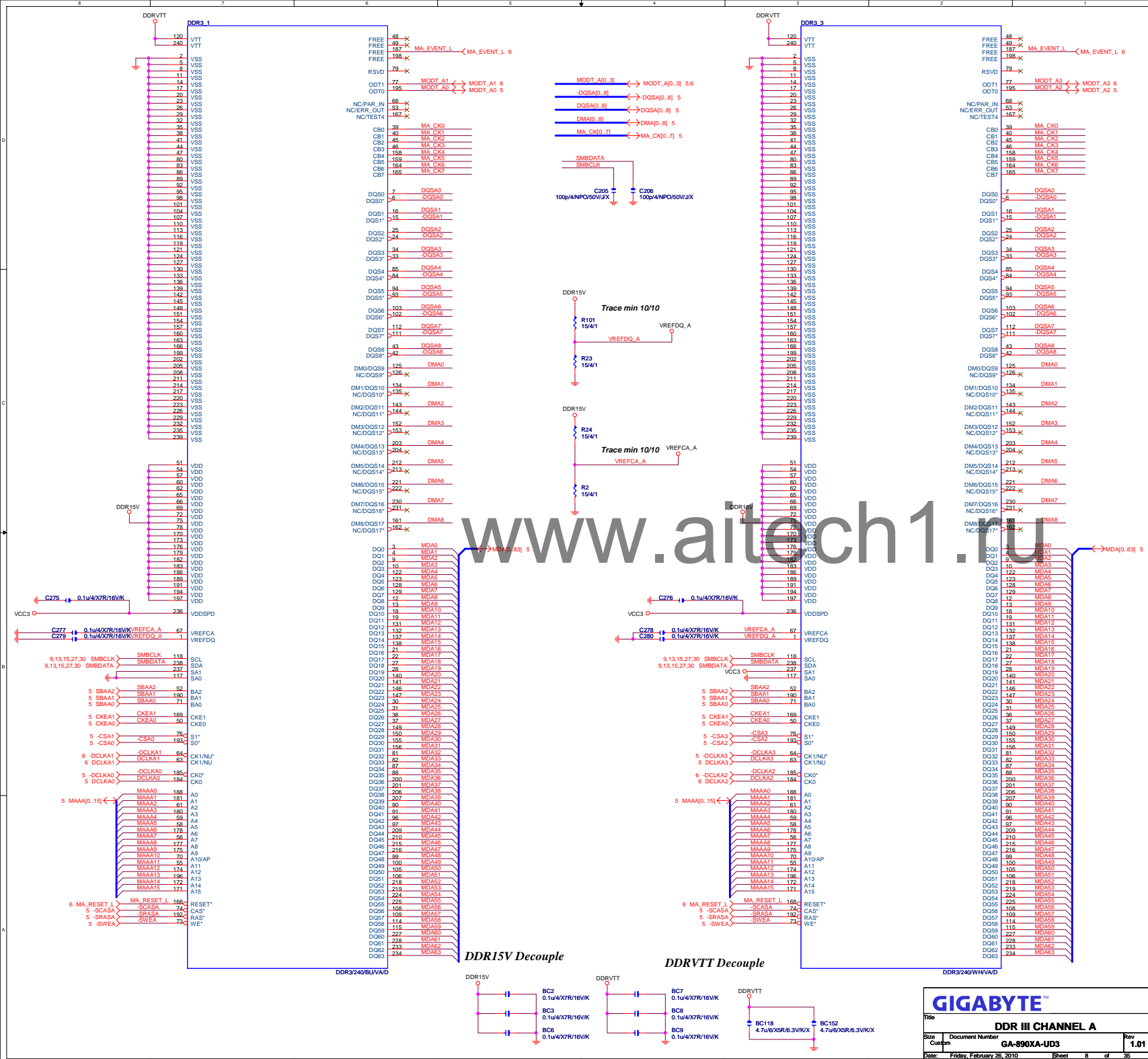
MEM CHA

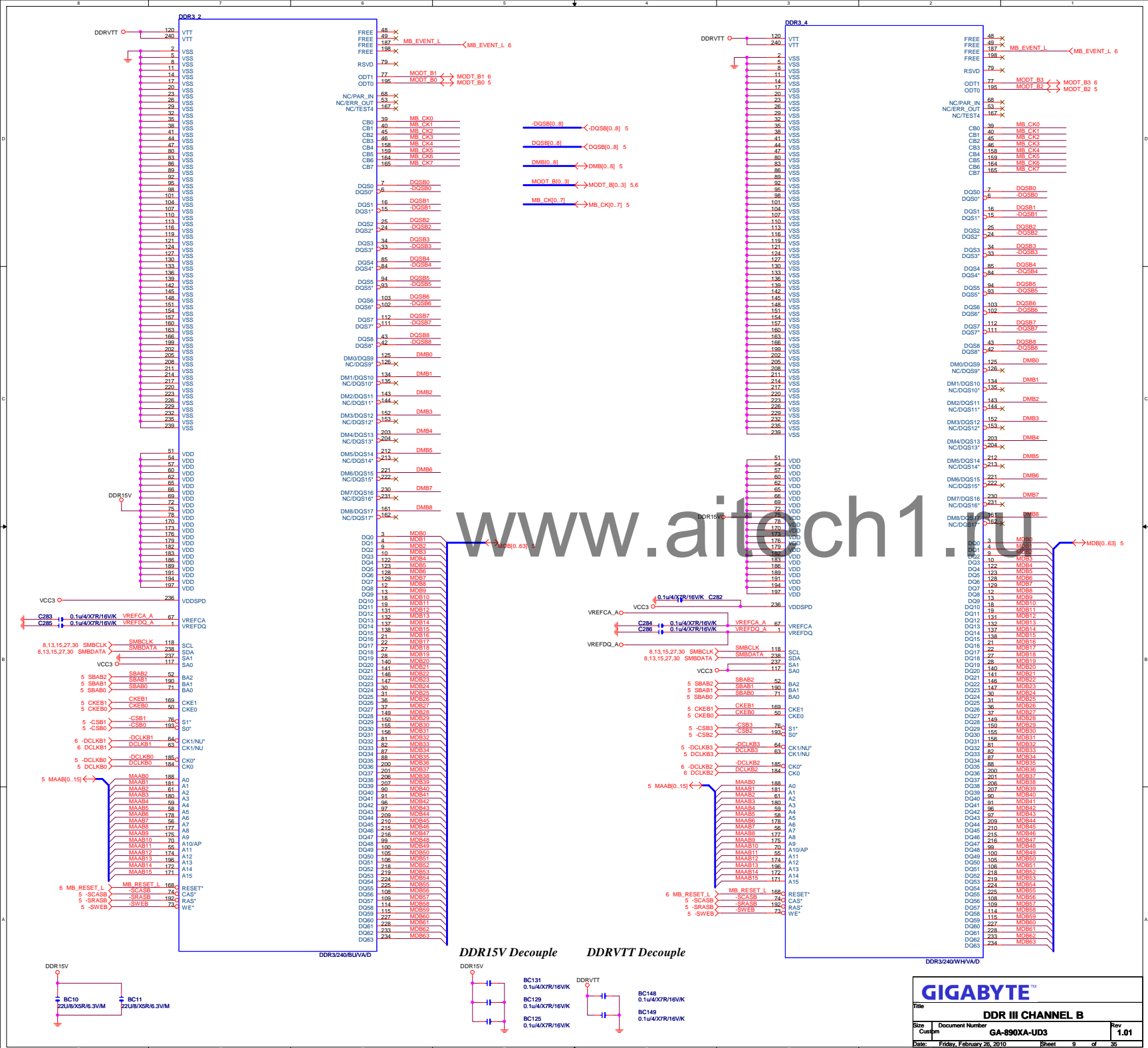


MEM CHB



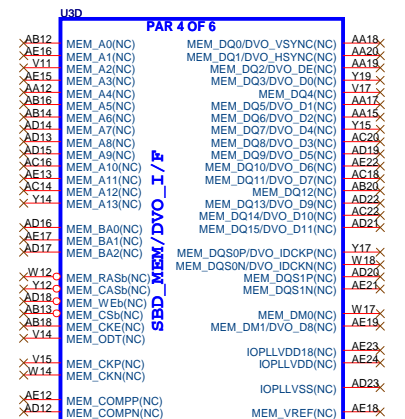
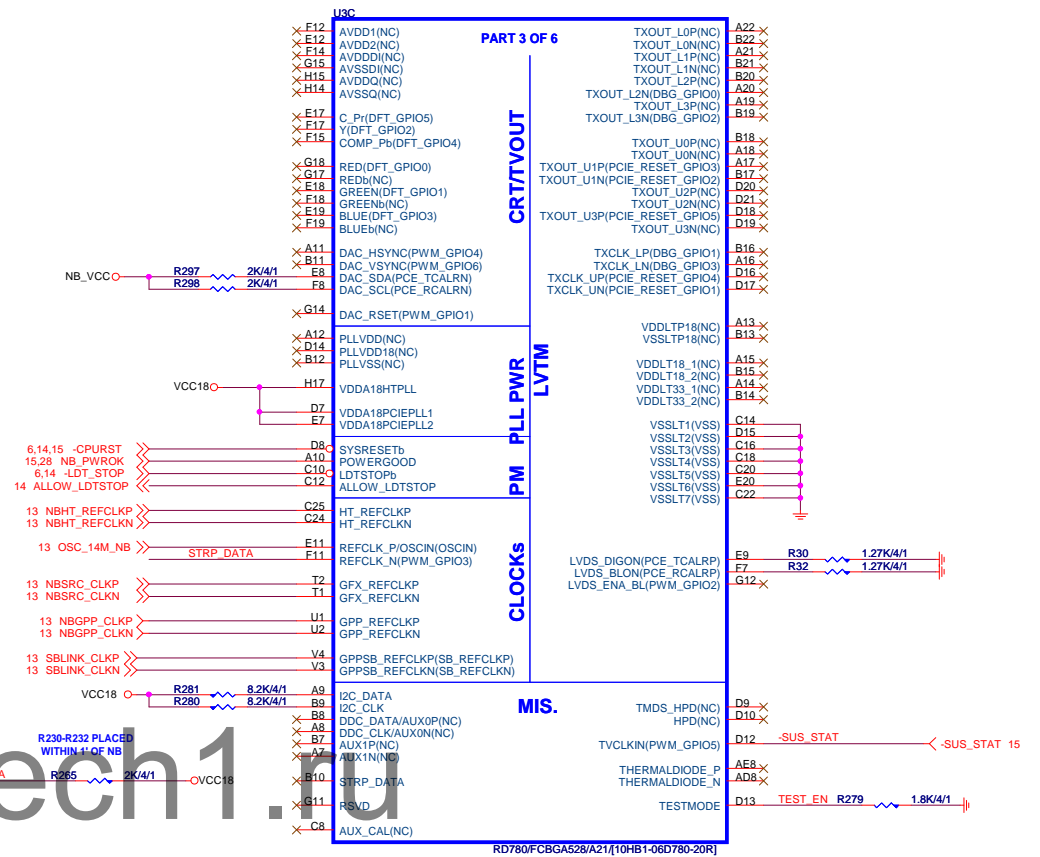
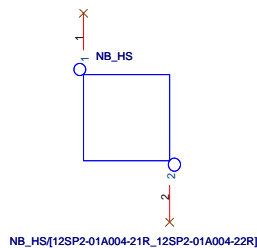
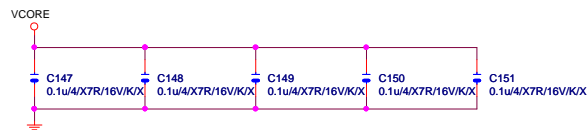
GIGABYTE™			
CPU DDR3 MEMORY			
Title	CPU DDR3 MEMORY		
Size	Document Number	Rev	
Custom	GA-890XA-UD3	1.01	
Date:	Friday, February 26, 2010	Sheet	5 of 35

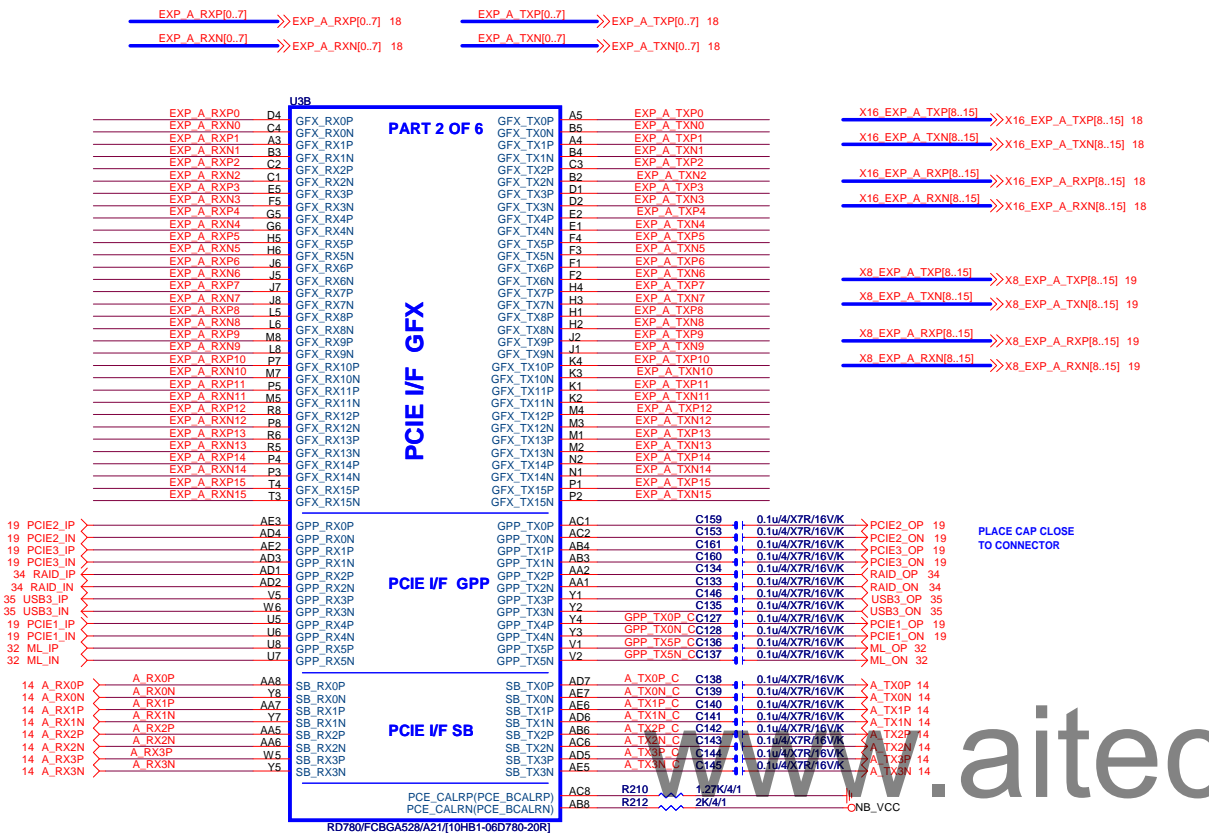




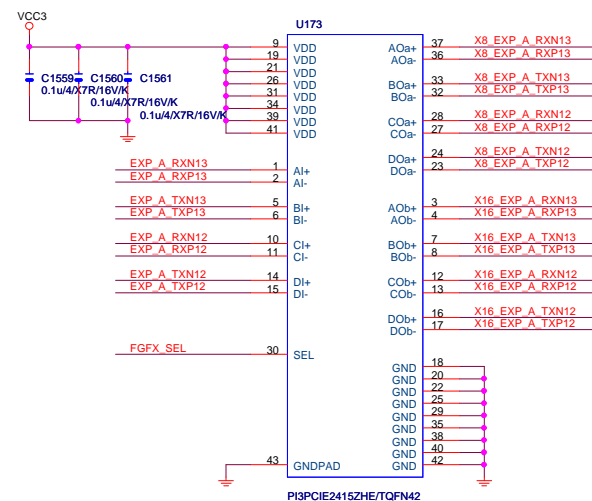
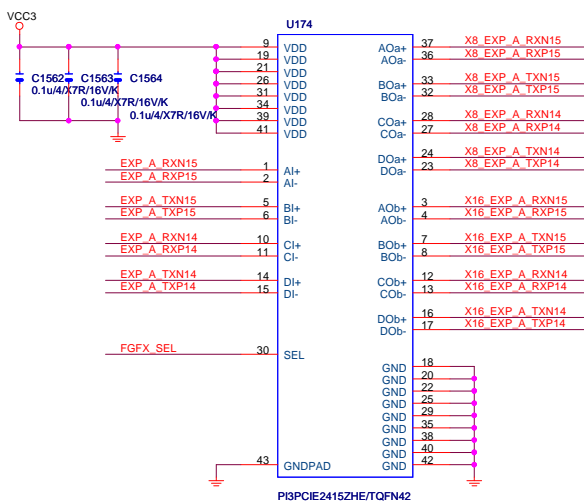
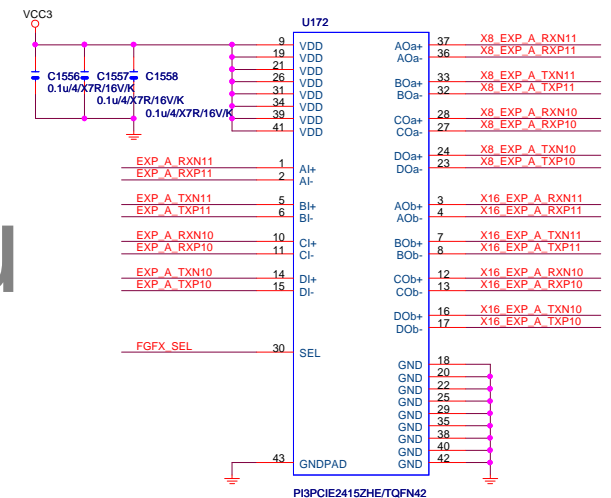
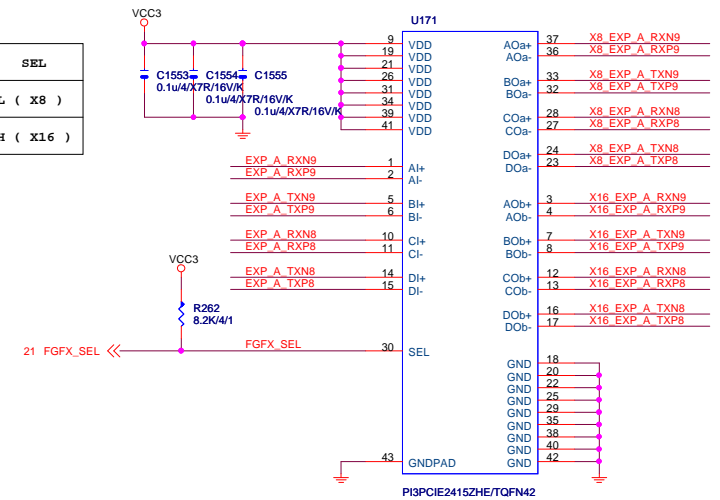


L0 CADIN_L[0..15] < L0 CADIN_L[0..15] 4
L0 CADIN_H[0..15] < L0 CADIN_H[0..15] 4
L0 CADOUT_L[0..15] < L0 CADOUT_L[0..15] 4
L0 CADOUT_H[0..15] < L0 CADOUT_H[0..15] 4



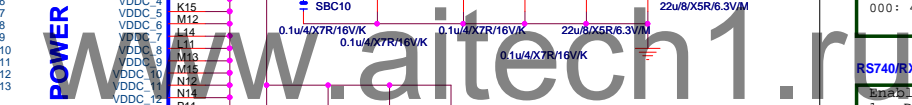


Function	SEL
xI--> x0a	L (X8)
xI--> x0b	H (X16)





RD780/FCBGA528/A21/[10HB1-06D780-20R]



PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: 4-0-0-0-0-0 Config A (register default to Config E)      default
110: 4-0-0-0-0-0 Config A
101: 4-4-0-0-0-0 Config B
100: 4-2-2-0-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780 DFT GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0]
(configure thru register setting)

(Configure this register setting)		default
1-1-1-1-1-1	Mode L	
1-1-1-1-1-1	Mode L	
2-0-2-0-2-0	Mode C2	
2-0-2-0-1-1	Mode K	
2-0-1-1-1-1	Mode E	
1-1-1-1-1-1	Mode L	
4-0-0-0-1-1	Mode C	
4-0-0-0-2-0	Mode B	

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

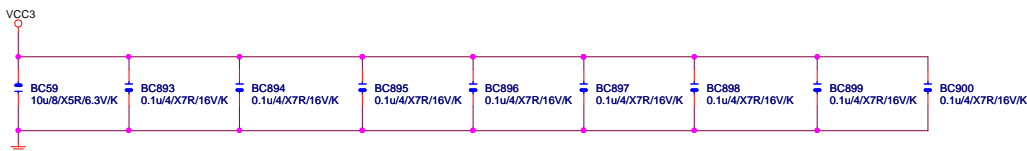
```

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable

```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
    thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
    setting only
RS740: Not supported
```

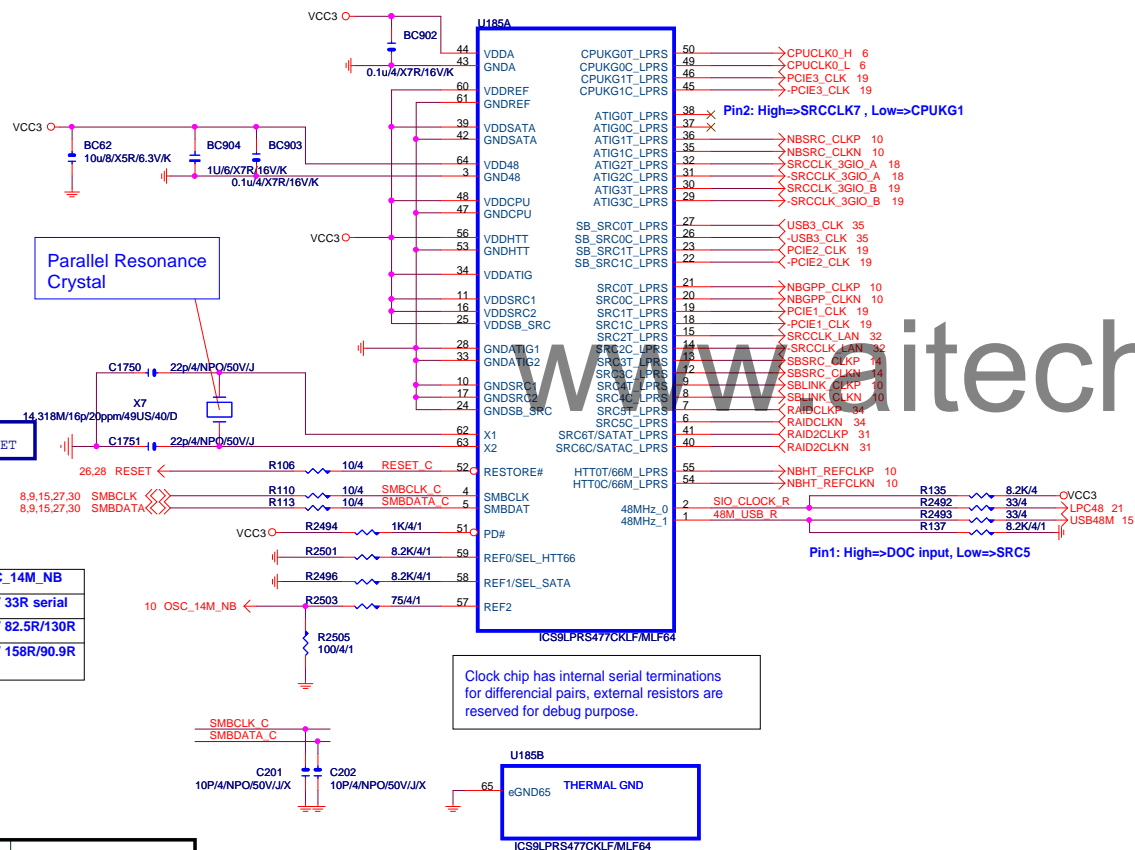
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

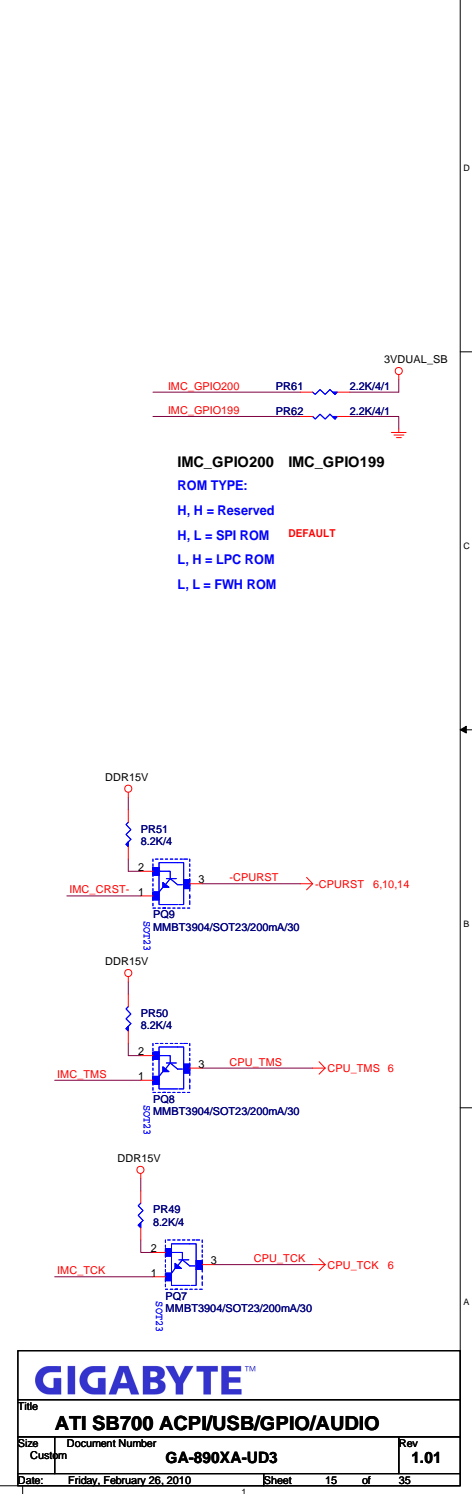
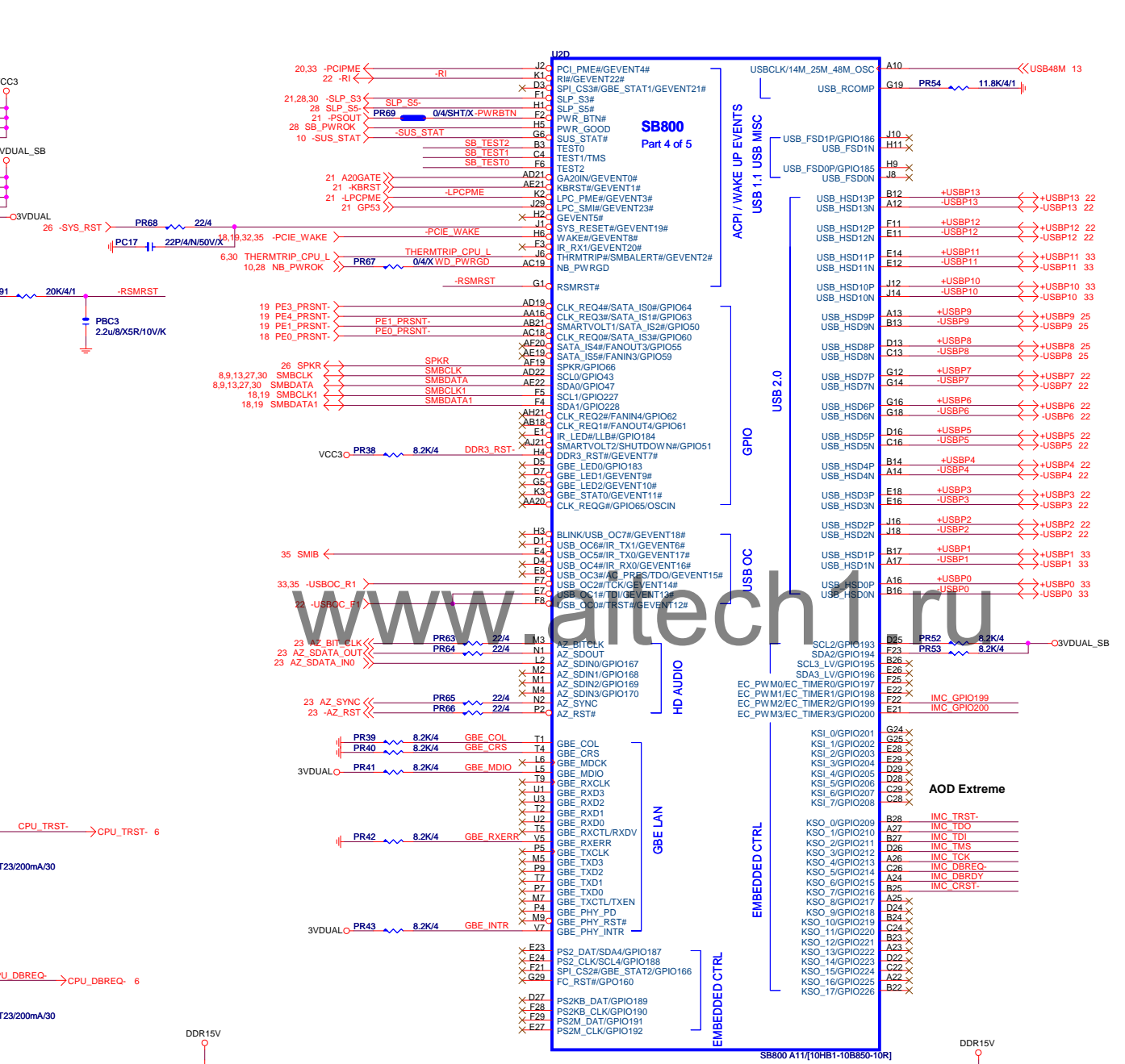
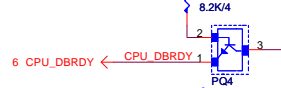
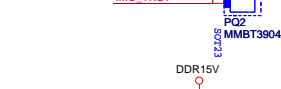
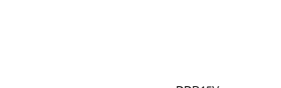
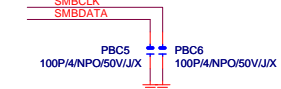
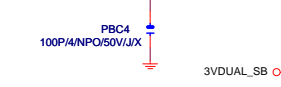
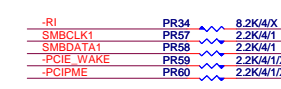
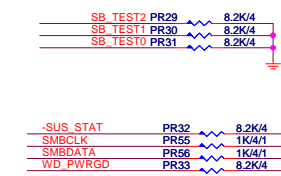
* the GFX_REFCLK input is required for all cases



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK





PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SB

PR75

PR74

1K4/1

9314/1

SATA_CALRP

SATA_CALRN

AB14

AA14

SATA_CALRP

SATA_CALRN

AD11

SATA_ACT#/GPIO67

AD16

SATA_X1

AC16

SATA_X2

PC42

22P/4/NPO/50V/J/X

PC43

22P/4/NPO/50V/J/X

SB_SPL DI

PR70

22/4

SB_SPL DO

PR71

22/4

SB_SPL CLK

PR72

22/4

SB_SPL CS_ITE

PR73

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SB_SPL CS_ITE

PR73

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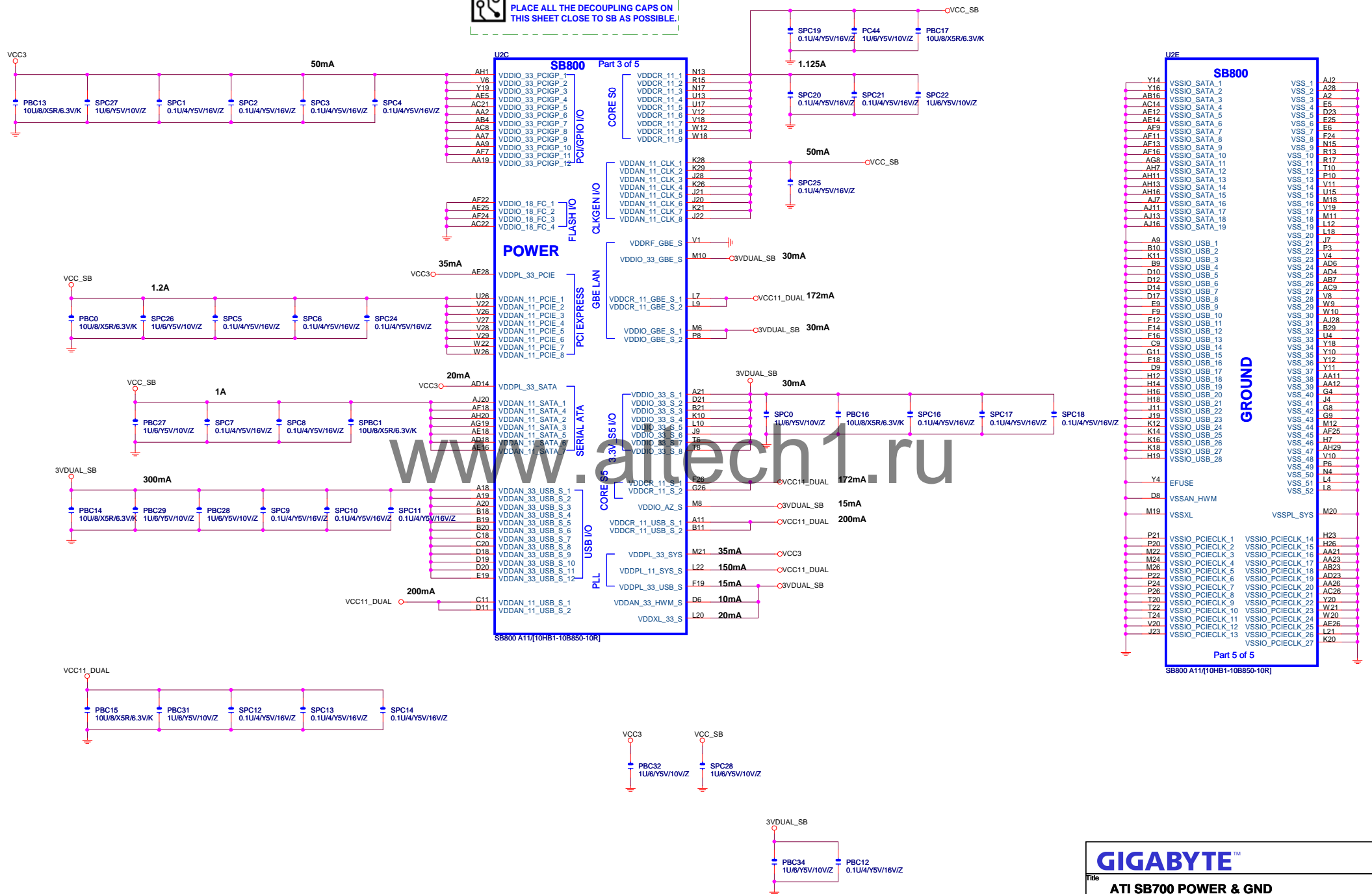
SB_SPL CS_ITE

PR73

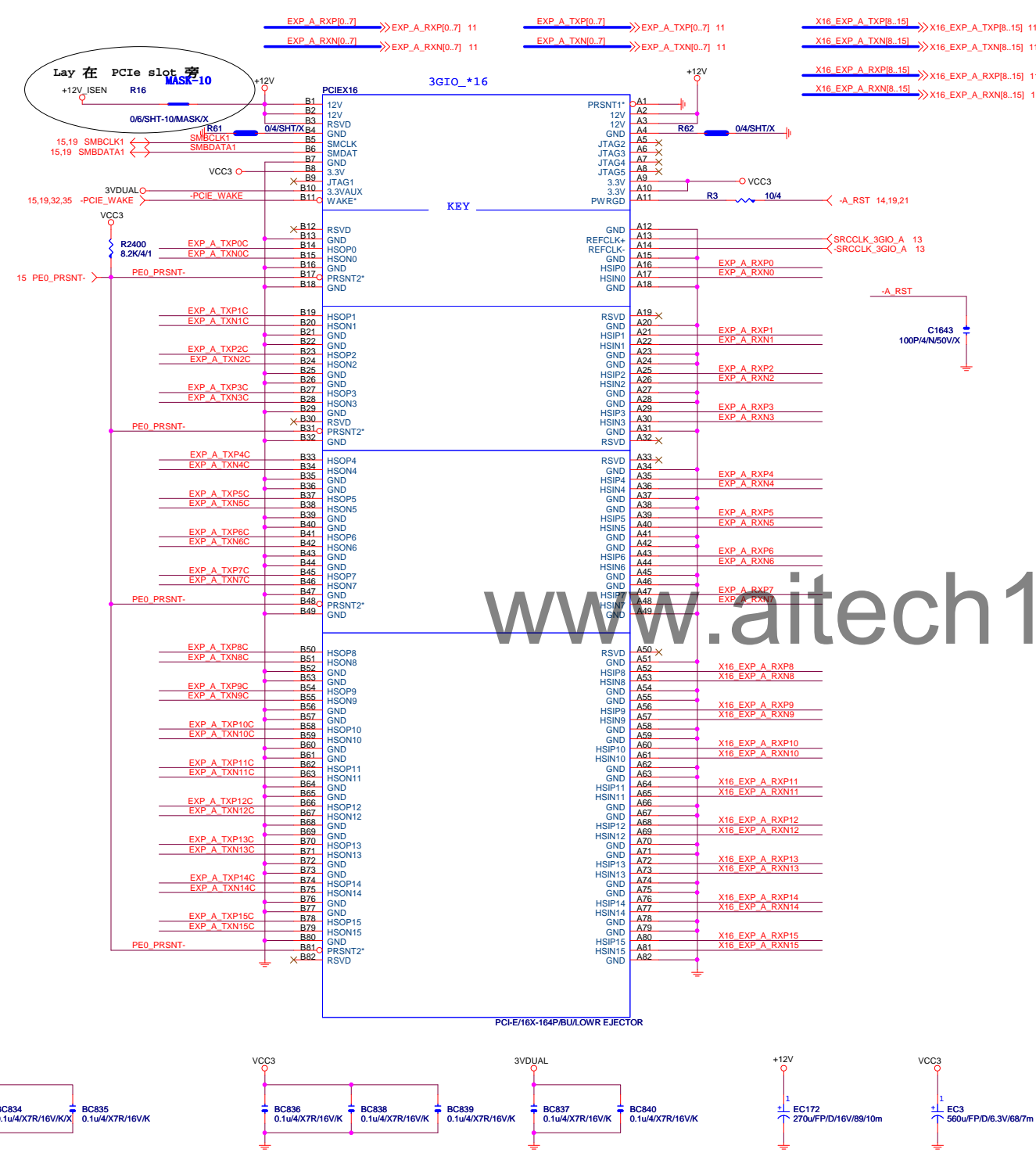
22/4



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



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EXP A TXP0	C1644	0.1u/4X7R/16V/K	EXP A TXP0C
EXP A TXN0	C1645	0.1u/4X7R/16V/K	EXP A TXN0C
EXP A TXP1	C1646	0.1u/4X7R/16V/K	EXP A TXP1C
EXP A TXN1	C1647	0.1u/4X7R/16V/K	EXP A TXN1C
EXP A TXP2	C1648	0.1u/4X7R/16V/K	EXP A TXP2C
EXP A TXN2	C1649	0.1u/4X7R/16V/K	EXP A TXN2C
EXP A TXP3	C1650	0.1u/4X7R/16V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1u/4X7R/16V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1u/4X7R/16V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1u/4X7R/16V/K	EXP A TXN4C
EXP A TXP5	C1654	0.1u/4X7R/16V/K	EXP A TXP5C
EXP A TXN5	C1655	0.1u/4X7R/16V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1u/4X7R/16V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1u/4X7R/16V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1u/4X7R/16V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1u/4X7R/16V/K	EXP A TXN7C
X16 EXP A TXP8	C1660	0.1u/4X7R/16V/K	EXP A TXP8C
X16 EXP A TXN8	C1661	0.1u/4X7R/16V/K	EXP A TXN8C
X16 EXP A TXP9	C1662	0.1u/4X7R/16V/K	EXP A TXP9C
X16 EXP A TXN9	C1663	0.1u/4X7R/16V/K	EXP A TXN9C
X16 EXP A TXP10	C1664	0.1u/4X7R/16V/K	EXP A TXP10C
X16 EXP A TXN10	C1665	0.1u/4X7R/16V/K	EXP A TXN10C
X16 EXP A TXP11	C1666	0.1u/4X7R/16V/K	EXP A TXP11C
X16 EXP A TXN11	C1667	0.1u/4X7R/16V/K	EXP A TXN11C
X16 EXP A TXP12	C1668	0.1u/4X7R/16V/K	EXP A TXP12C
X16 EXP A TXN12	C1669	0.1u/4X7R/16V/K	EXP A TXN12C
X16 EXP A TXP13	C1670	0.1u/4X7R/16V/K	EXP A TXP13C
X16 EXP A TXN13	C1671	0.1u/4X7R/16V/K	EXP A TXN13C
X16 EXP A TXP14	C1672	0.1u/4X7R/16V/K	EXP A TXP14C
X16 EXP A TXN14	C1673	0.1u/4X7R/16V/K	EXP A TXN14C
X16 EXP A TXP15	C1674	0.1u/4X7R/16V/K	EXP A TXP15C
X16 EXP A TXN15	C1675	0.1u/4X7R/16V/K	EXP A TXN15C

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PCI EXPRESS X 16 ,X1

Size

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Rev

Custom

GA-890XA-UD3

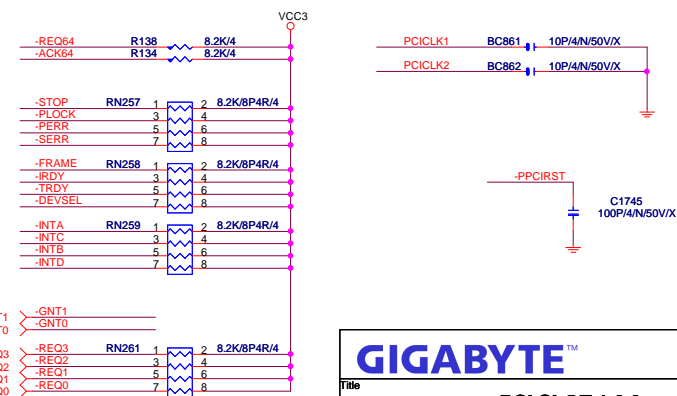
1.01

Date: Friday, February 26, 2010

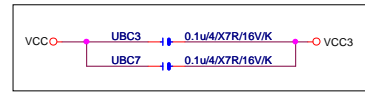
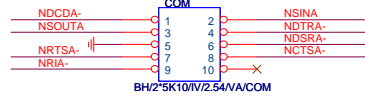
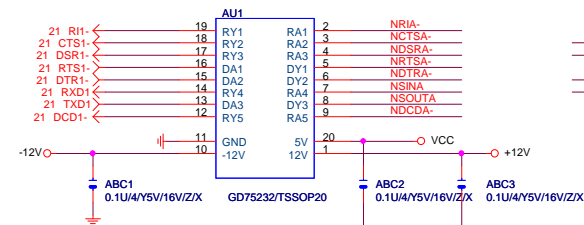
Sheet

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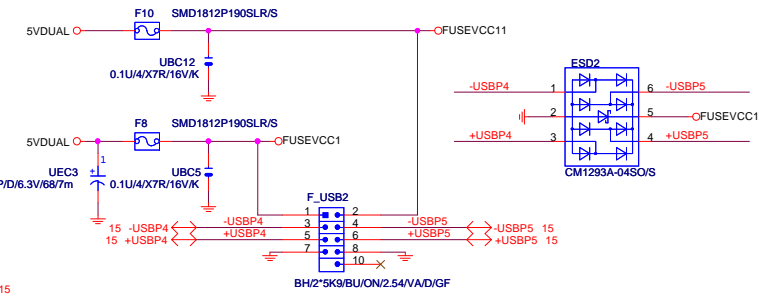
PCI SLOT2



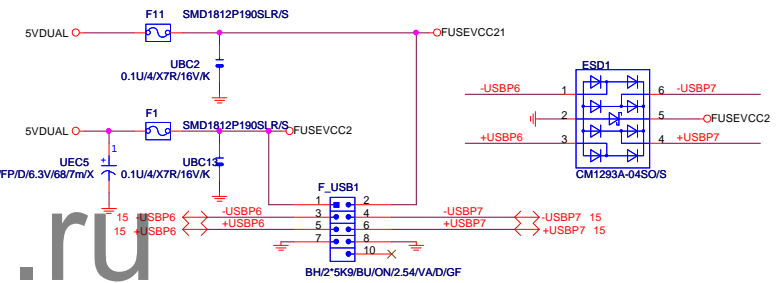
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PCI SLOT 1,2,3			
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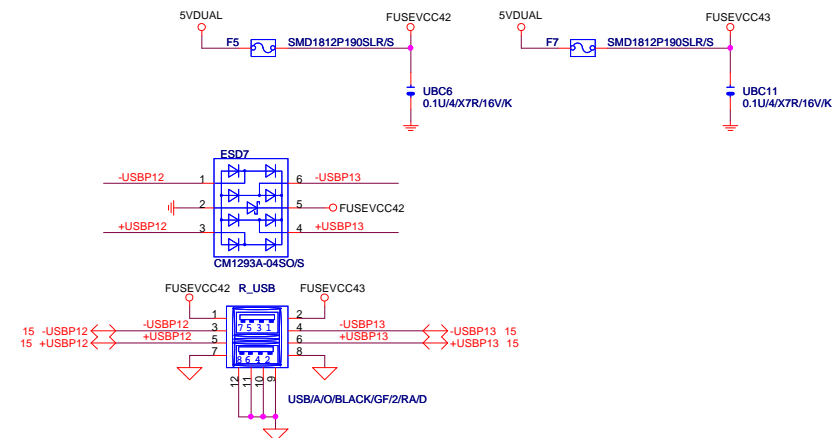
FRONT SIDE USB2



FRONT SIDE USB1



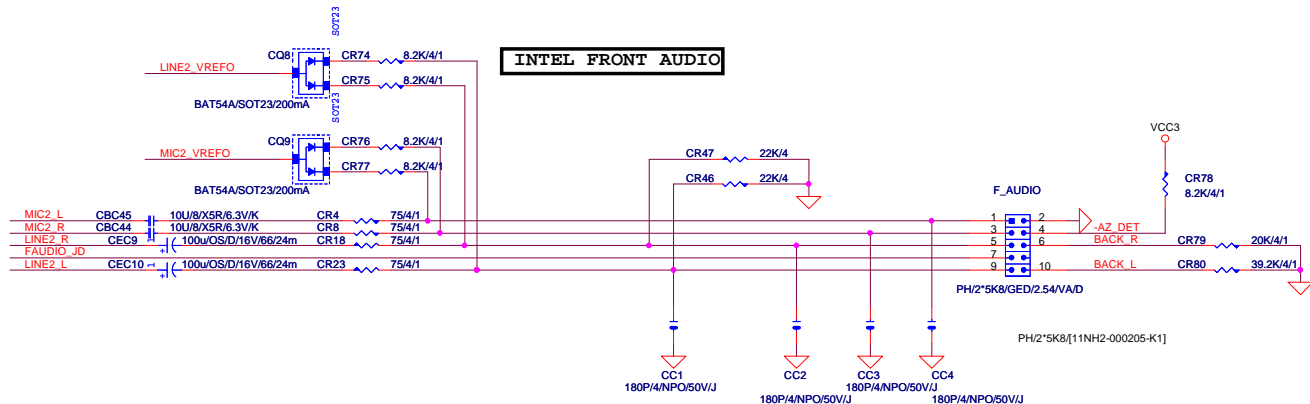
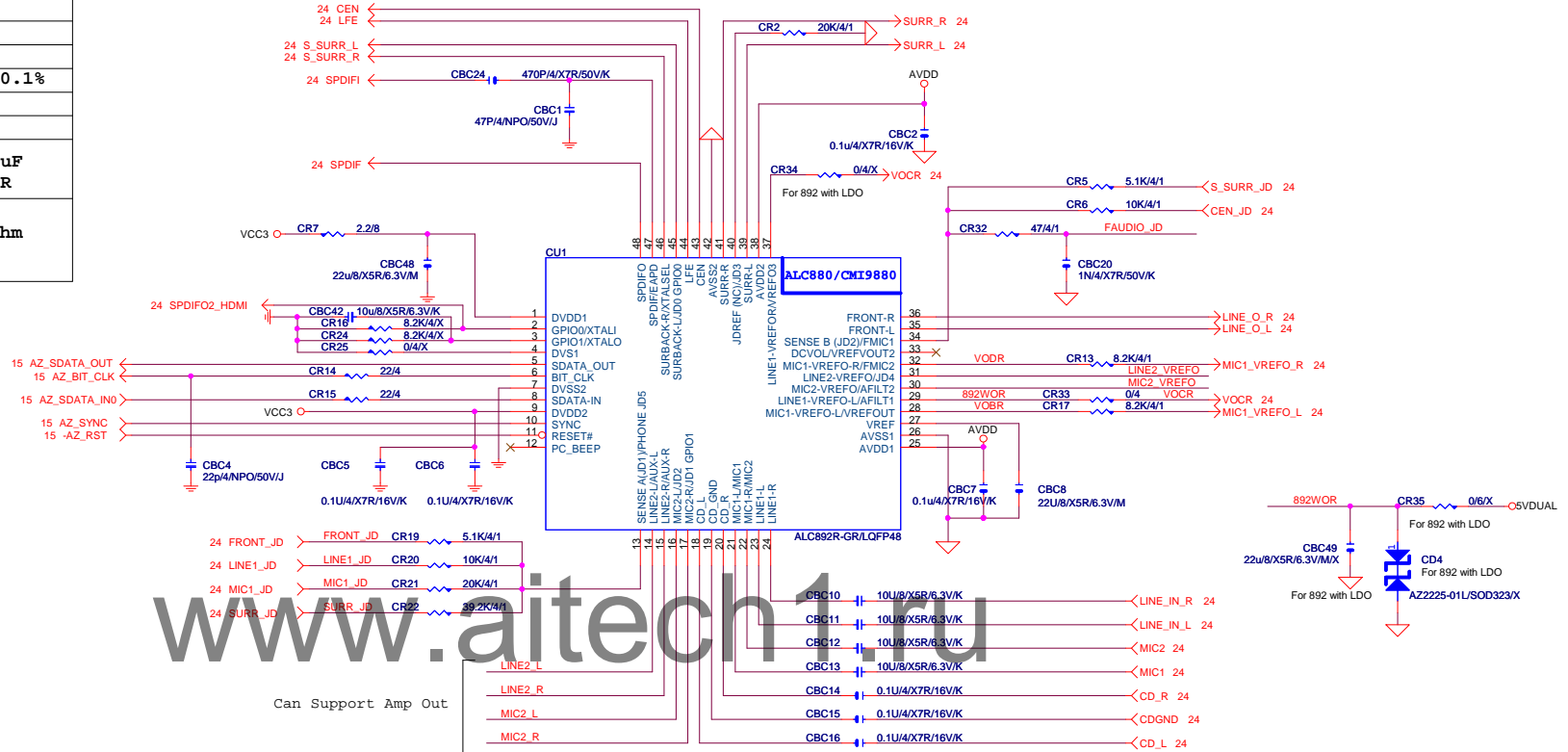
REAR USB

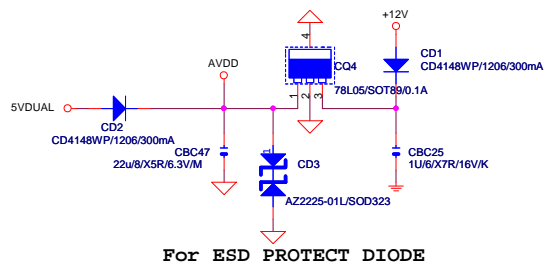
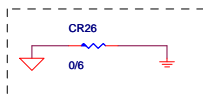


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Title	COM/LPT/F_USB		
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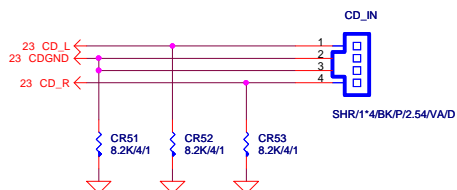
	ALC892	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



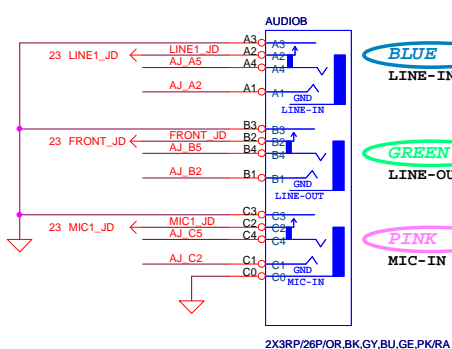
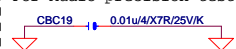


For ESD PROTECT DIODE

CD IN



For Audio precision test



BLUE
LINE-IN

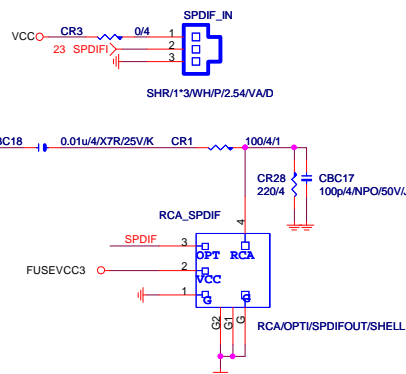
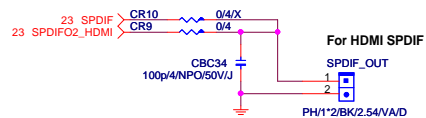
GREEN
LINE-OUT

PINK
MIC-IN

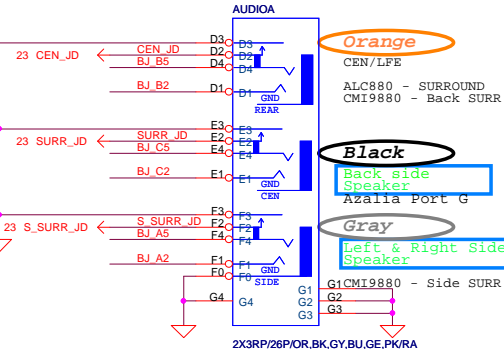
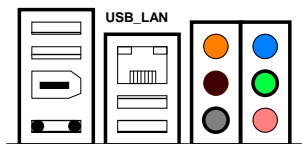
2X3RP/26P/0R,BK,GY,BU,GE,PK,RA

A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

SPDIF



USB_1394_ESATA



Orange
CEN/LFE

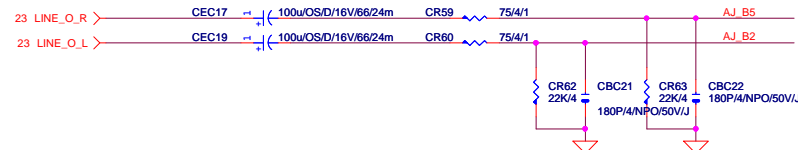
Black
Back side
Speaker

Gray
Left & Right Side
Speaker

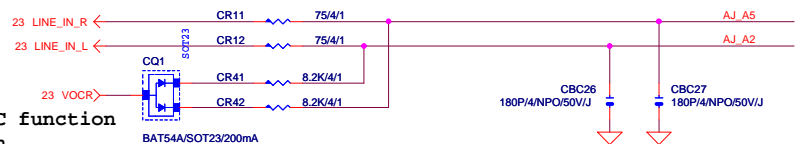
2X3RP/26P/0R,BK,GY,BU,GE,PK,RA

A3R7/13P/0BG/[11NR6-403006-71]
3R7+15P/[11NR6-403004-31]

LINE OUT FRONT OUT

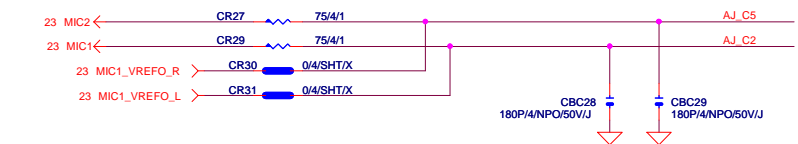


LINE-IN

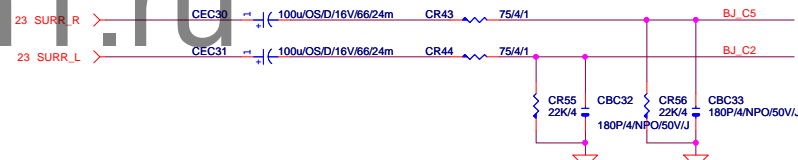


Verify MIC function
in LINE-in

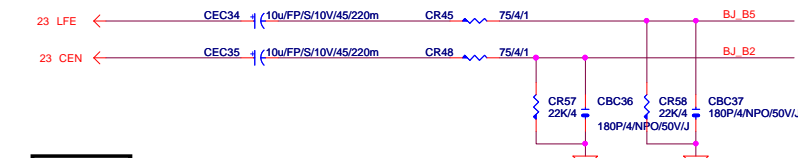
MIC



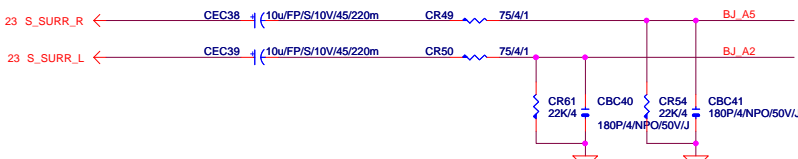
SURROUND



CEN/LFE



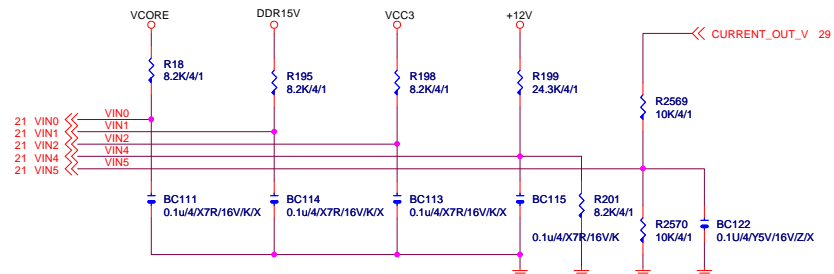
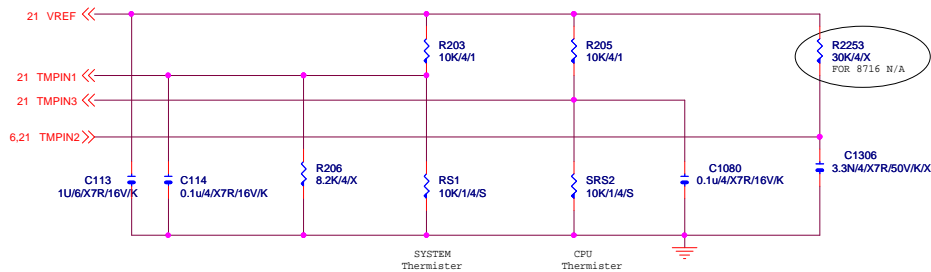
SURR BACK



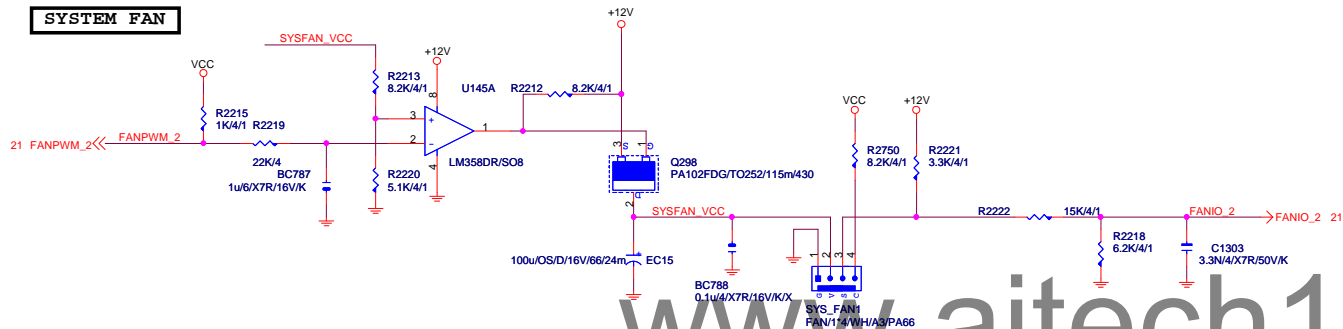
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Title		
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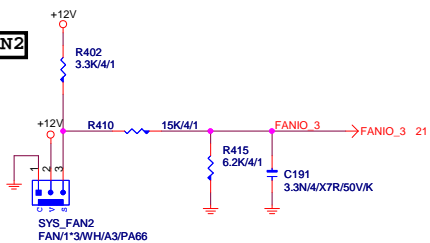
Hardware Monitor circuits



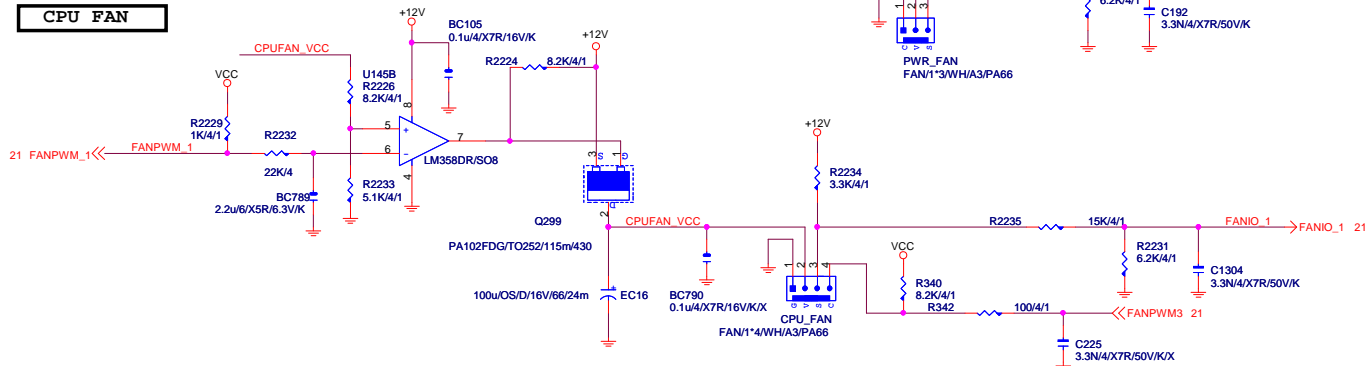
SYSTEM FAN



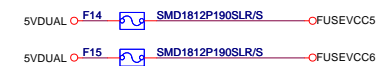
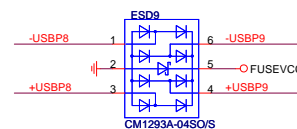
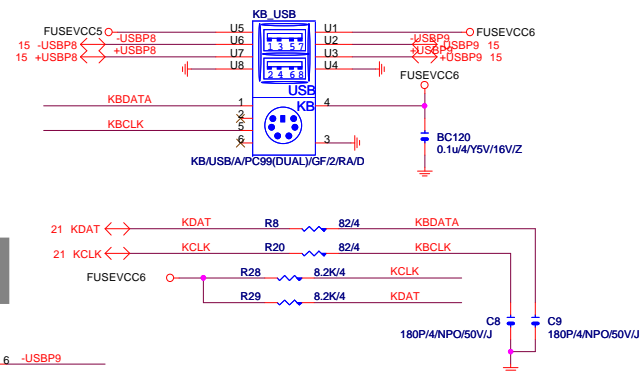
POWER FAN



CPU FAN

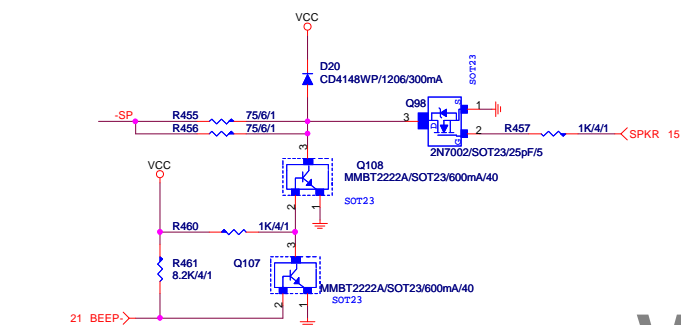
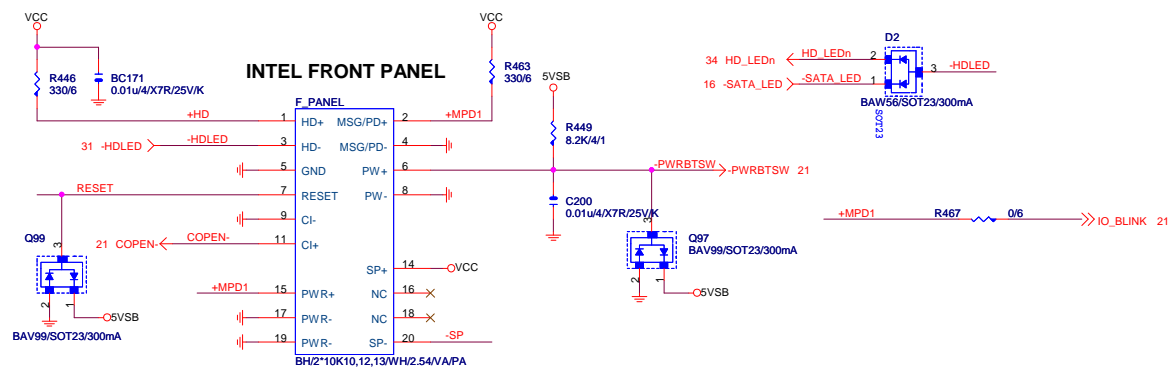


KB & USB

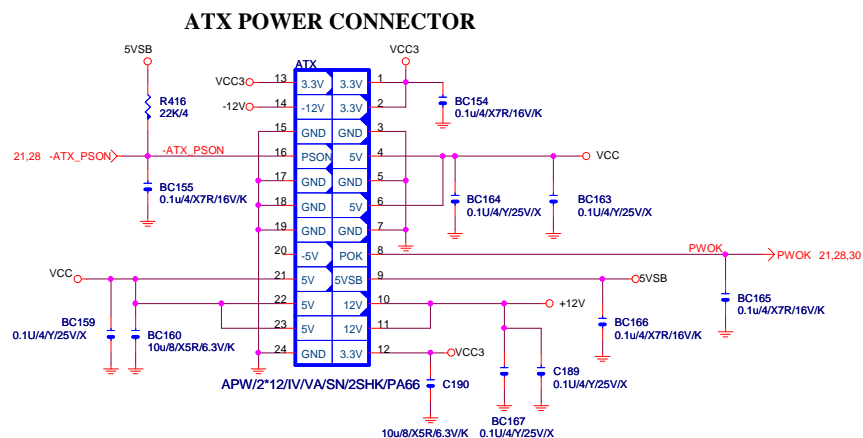


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Title			
FAN/HWMO KB/MS			
Size	Document Number	Rev	
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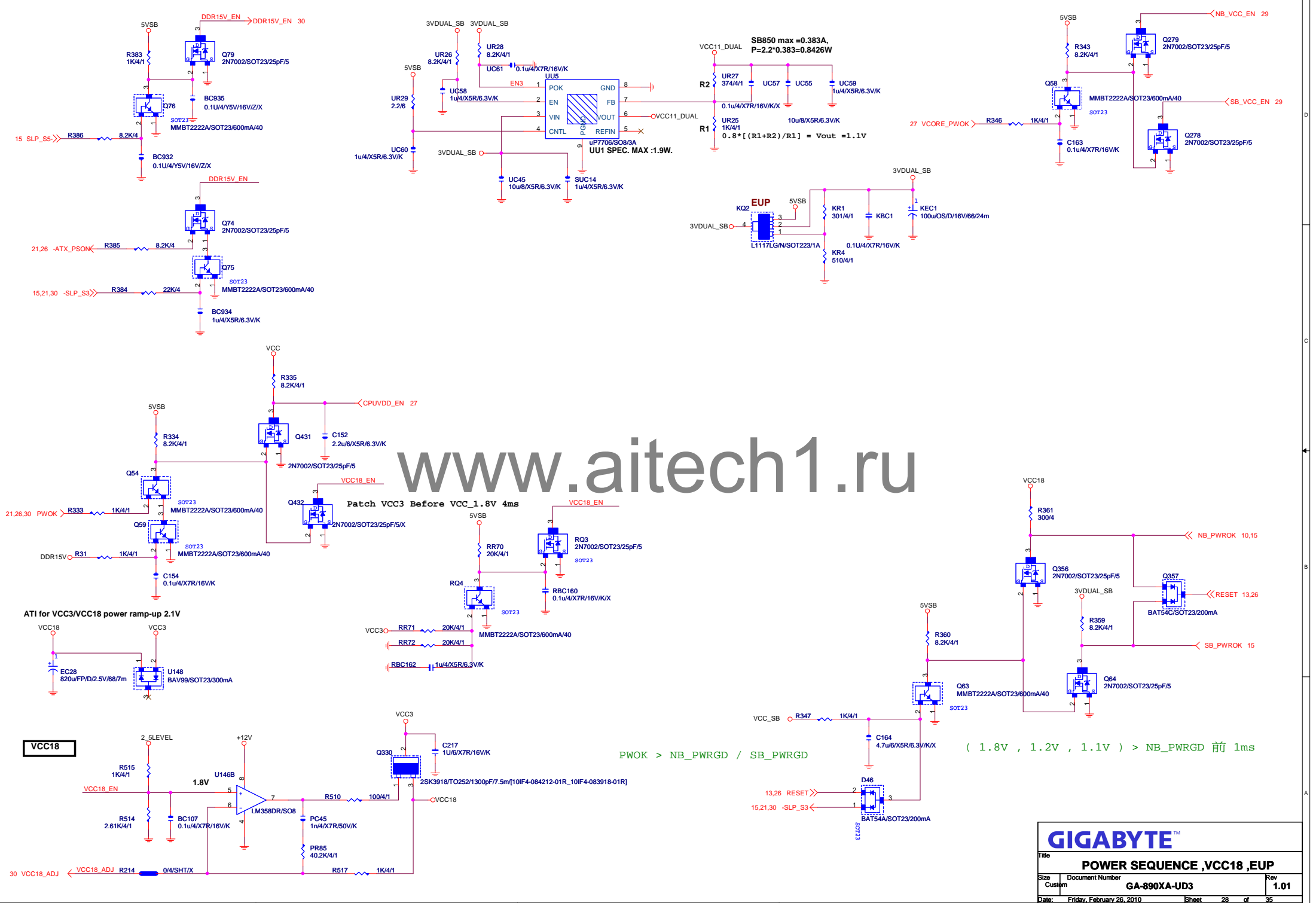


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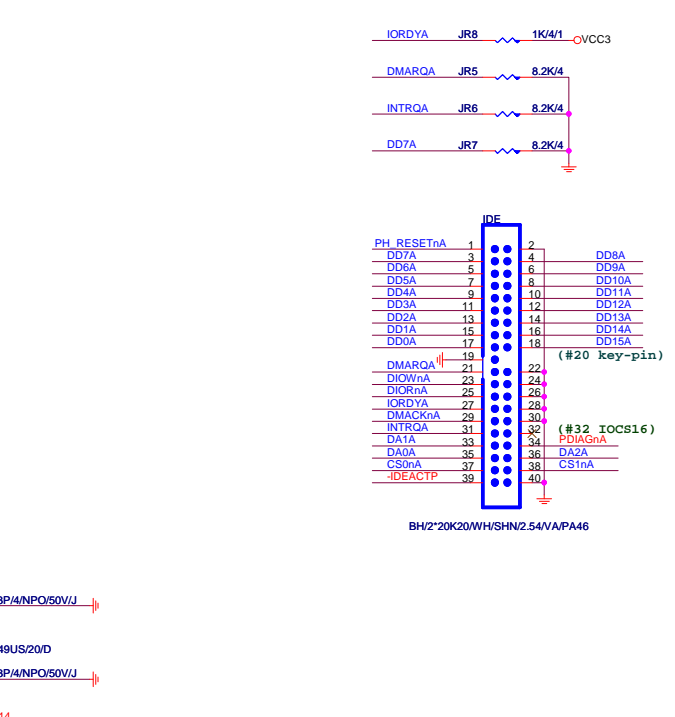
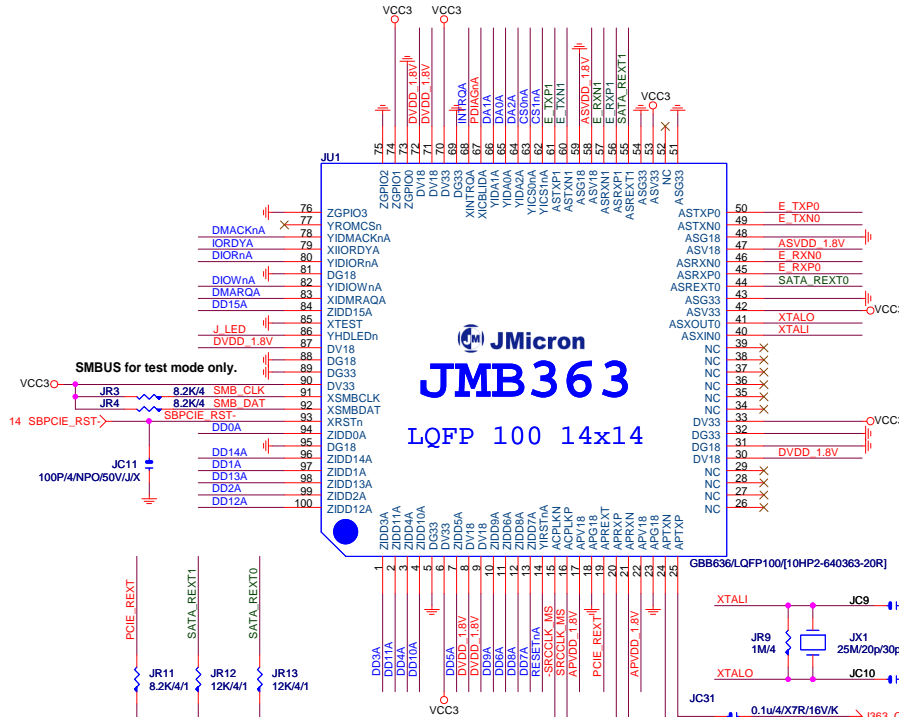
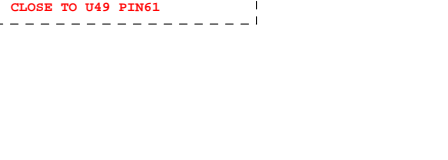
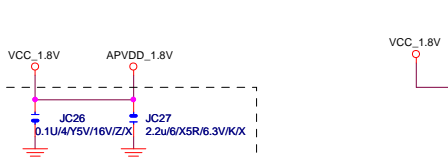
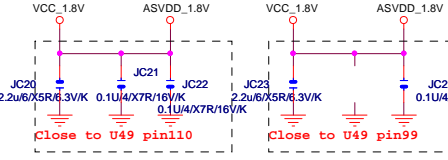
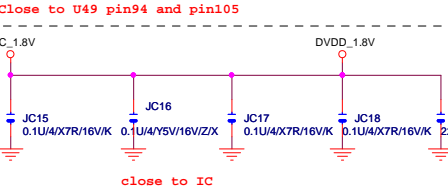
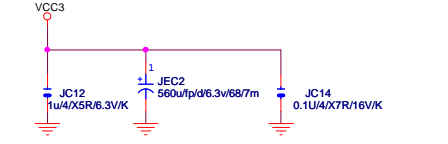
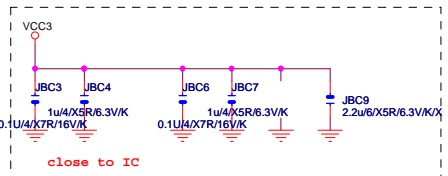
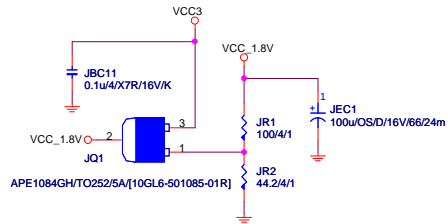


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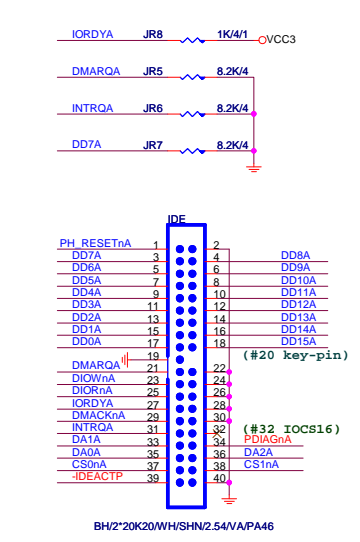
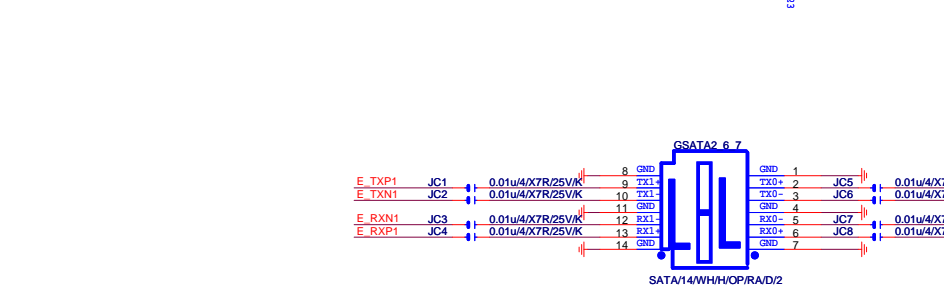
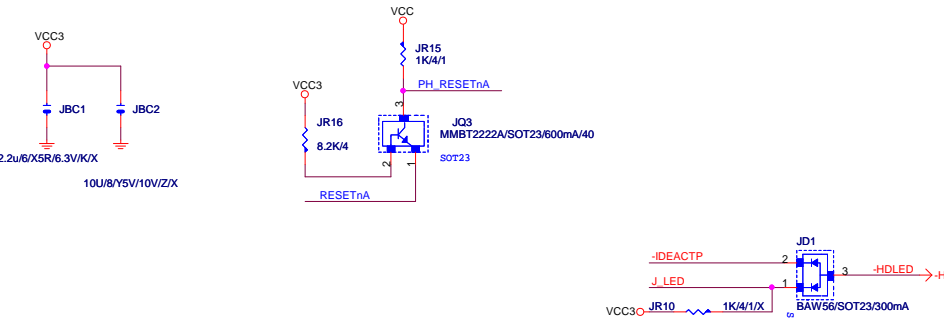
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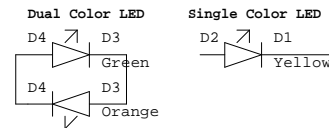
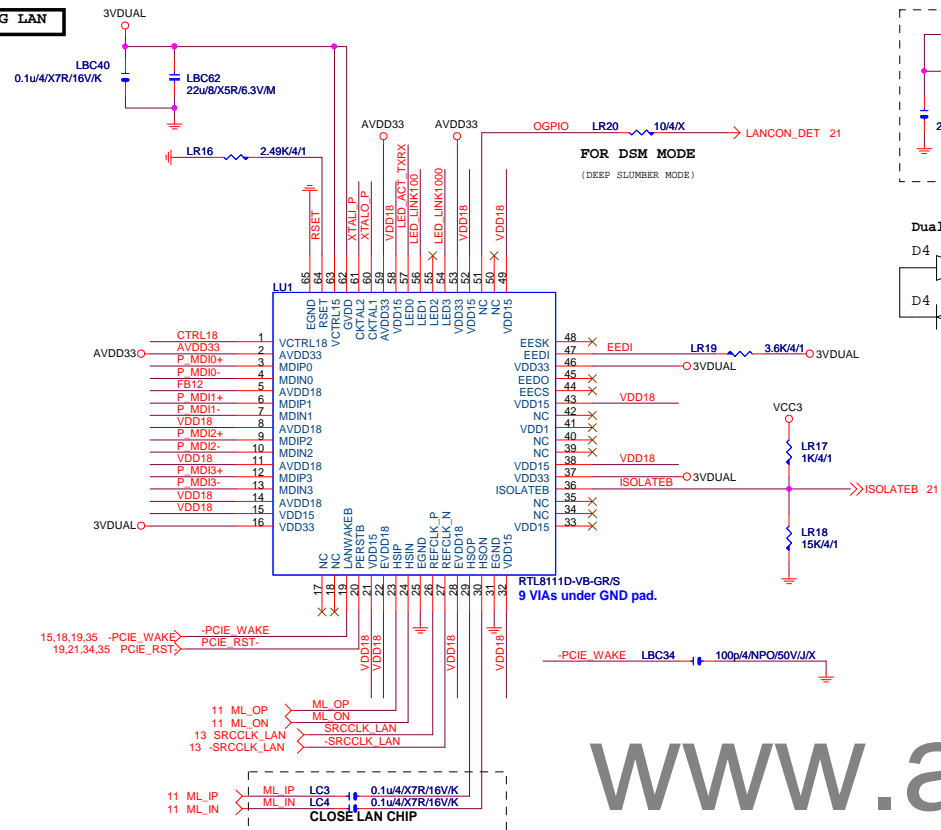
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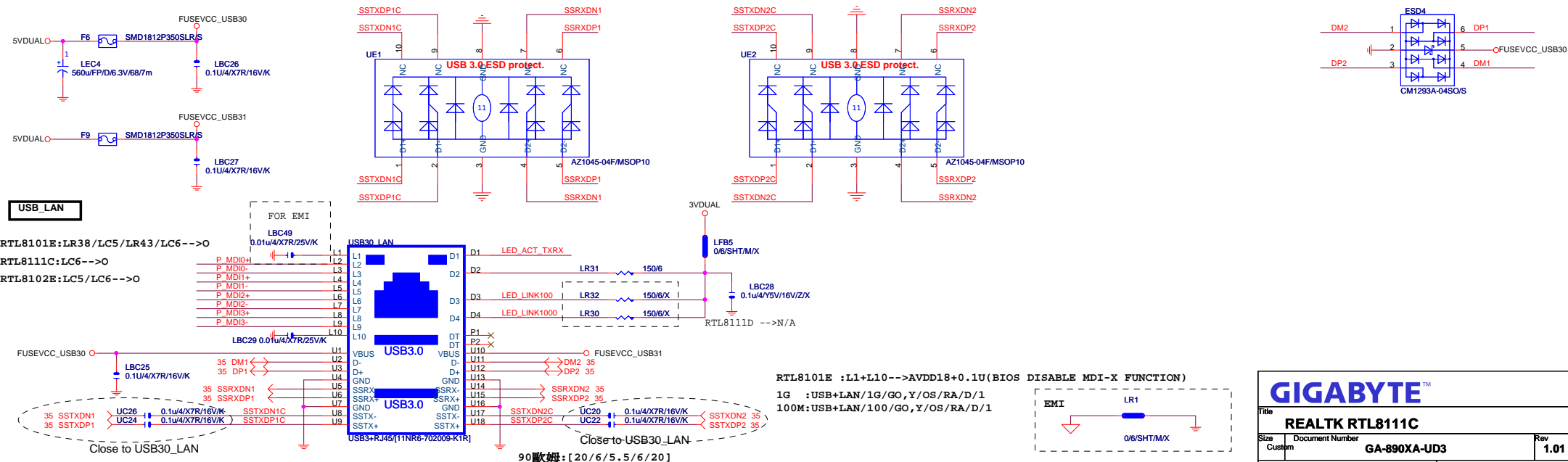
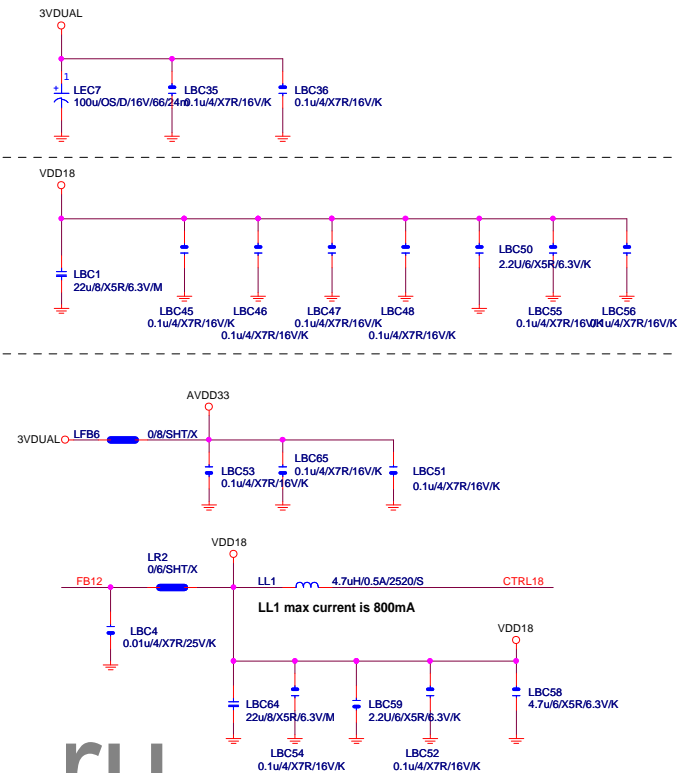
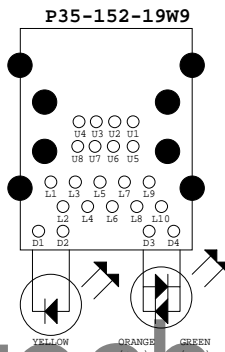
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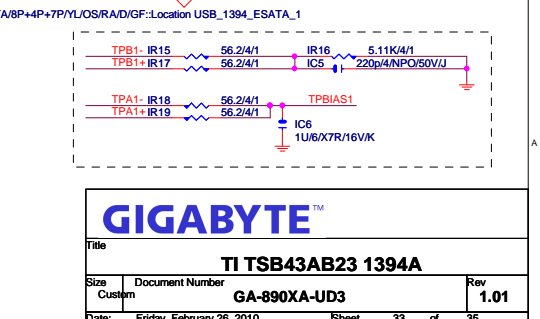
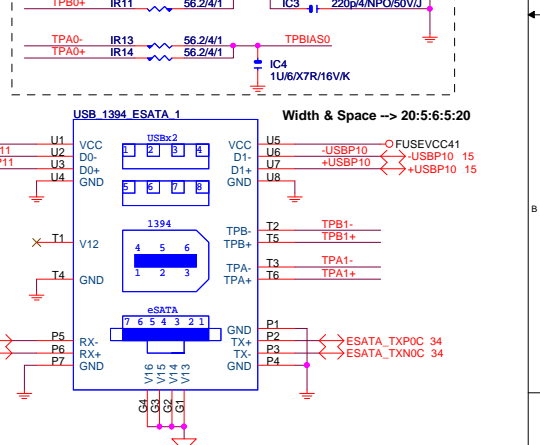
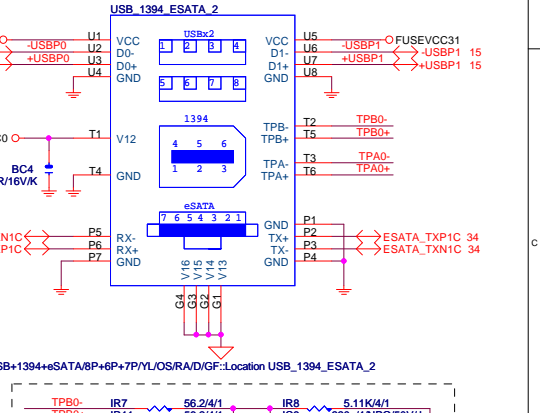
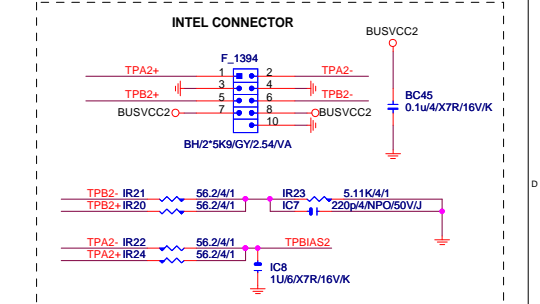
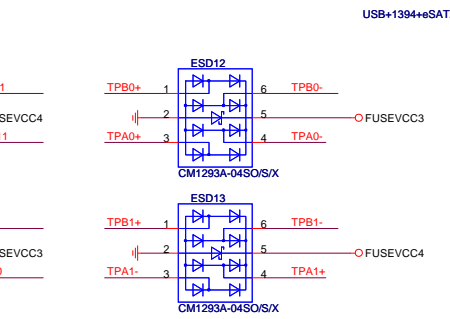
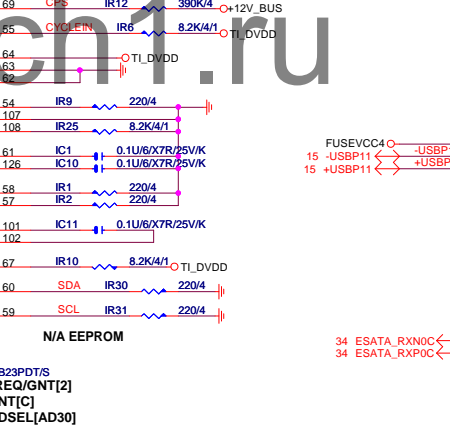
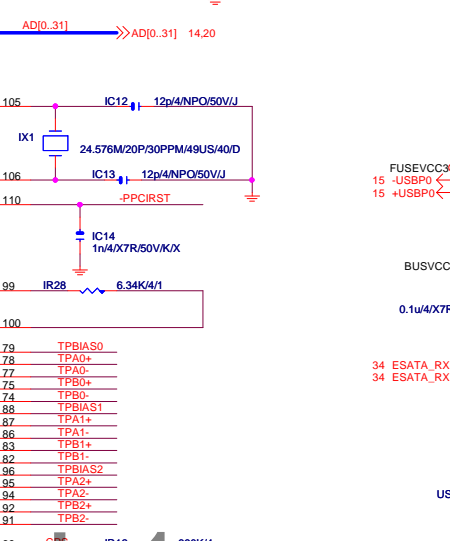
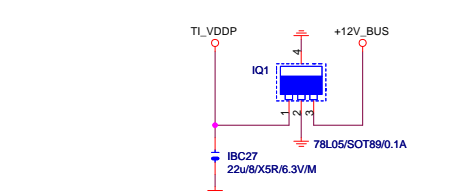
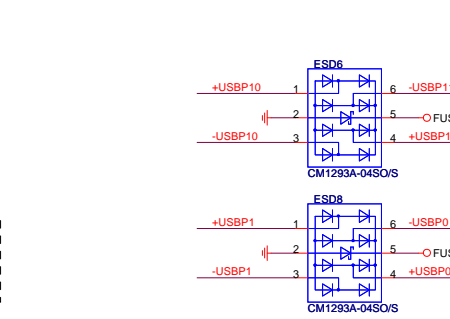
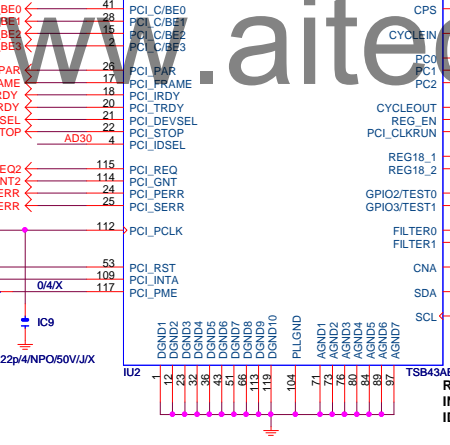
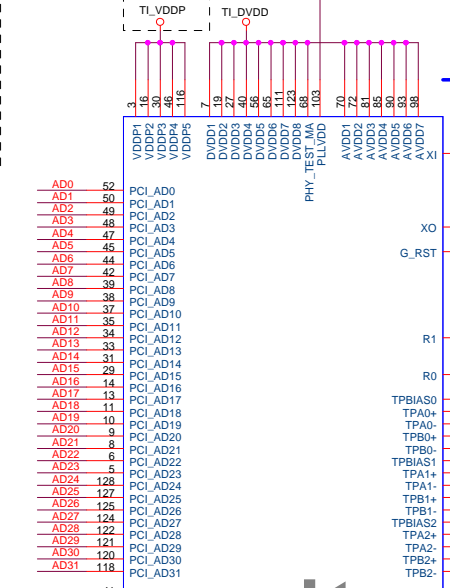
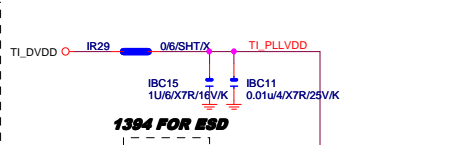
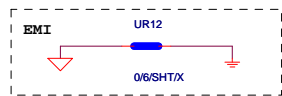
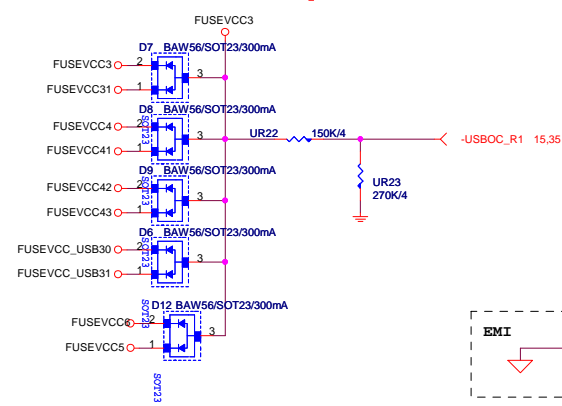
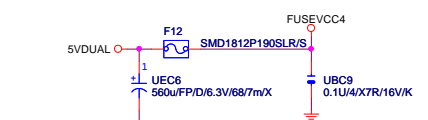
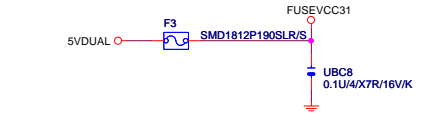
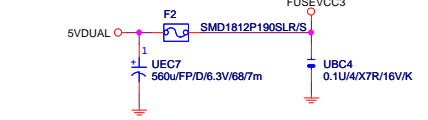
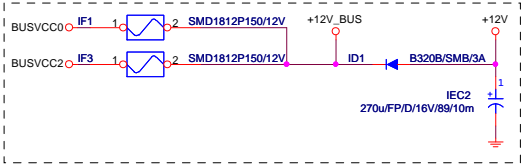
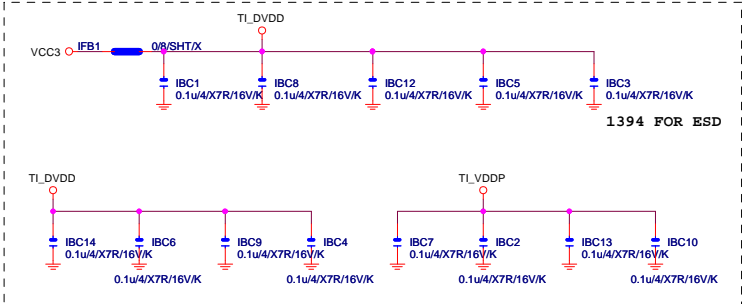
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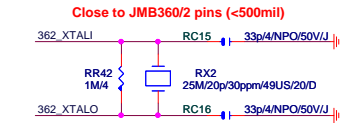
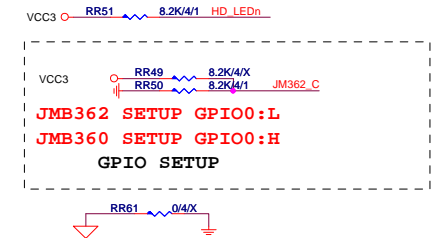
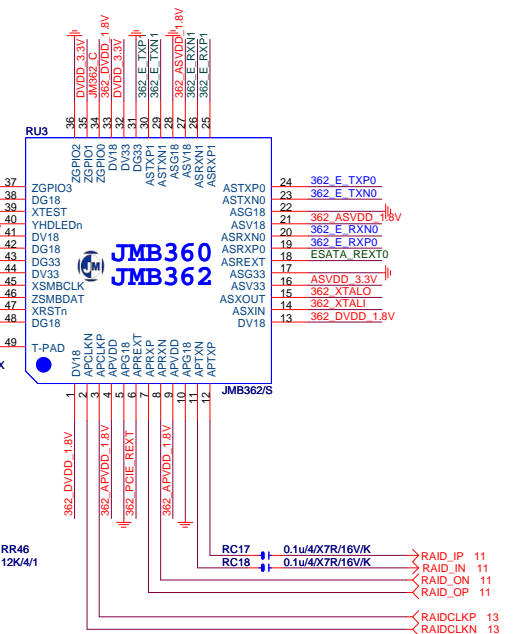
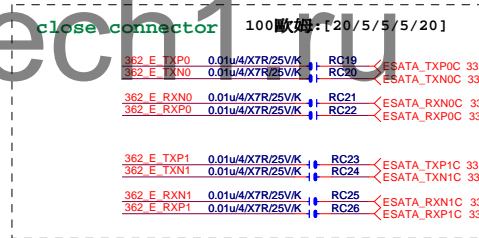
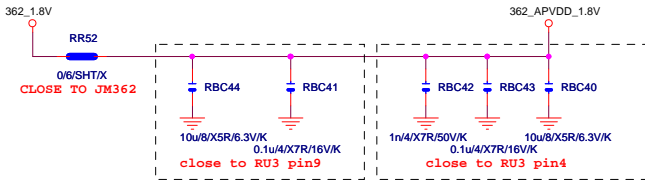
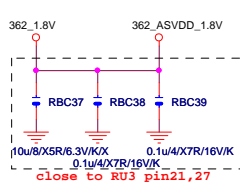
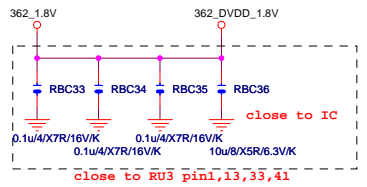
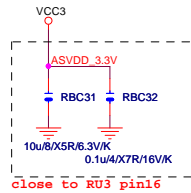
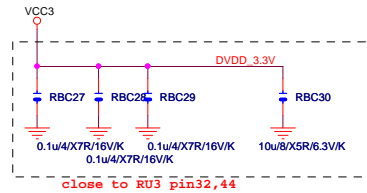
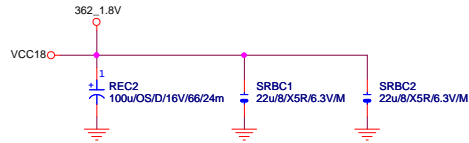


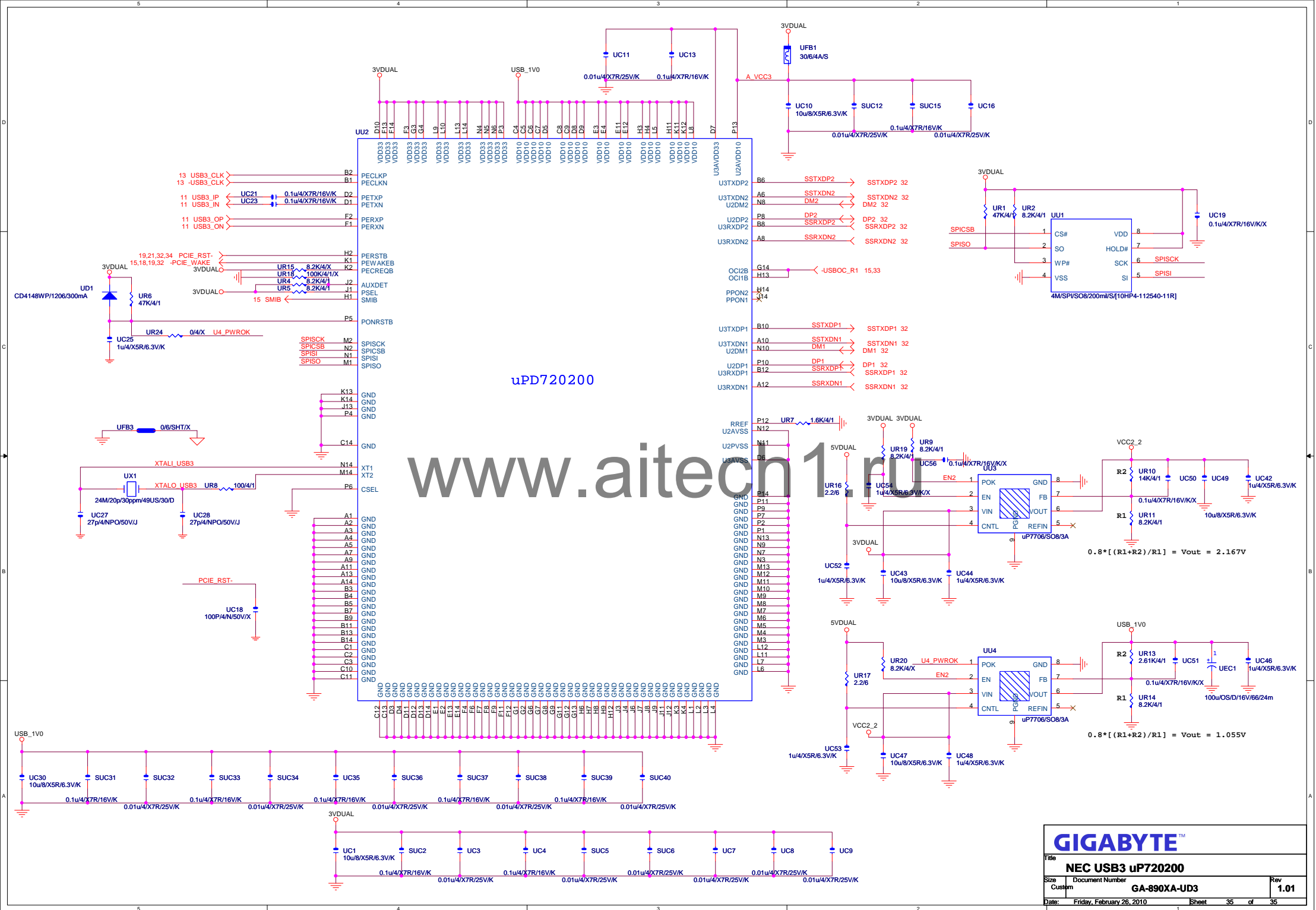
USB_LAN CONNECTOR



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Title
NEC USB3 uP720200

Size
Custom

Date: Friday, February 26, 2010

Document Number
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